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A Flexible Incremental Phase Servo With Digital Outputs For Indicating Phase and Doppler Frequency of Ionospherically Propagated Radio Signals

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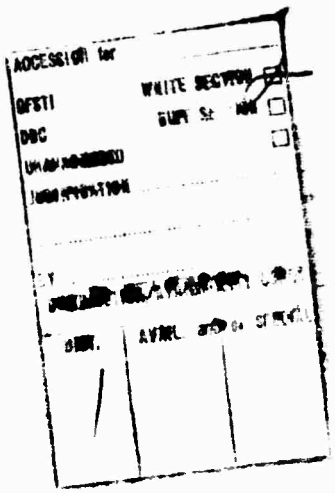

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A FLEXIBLE INCREMENTAL PHASE SERVO WITH DIGITAL OUTPUTS FOR INDICATING PHASE AND DOPPLER FREQUENCY OF IONOSPHERICALLY PROPAGATED RADIO SIGNALS

Richard N. Grubb

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A FLEXIBLE INCREMENTAL PHASE SERVO WITH DIGITAL OUTPUTS FOR INDICATING PHASE AND DOPPLER FREQUENCY OF IONOSPHERICALLY PROPAGATED RADIO SIGNALS

by

Richard N. Grubb

A flexible solid-state phase-tracking system designed for use on ionospherically propagated radio signals is described. The output is basically digital in form and suitable for use with automatic data processing systems. The unit provides an output equal to the rate of change of phase or Doppler frequency of the incoming signal and is sufficiently flexible to be used on VLF through HF signals. The design is described and specifications of the prototype unit included. Some examples of results obtained using the equipment are given.

KEY WORDS: Phase, Doppler, ionospheric, propagation, digital

1. INTRODUCTION

Radio signals propagated via the ionosphere experience changes in phase path length because of changes in the ionosphere. The latter are both regular, for example seasonal and diurnal as a direct result of solar control, and irregular, for example changes resulting from solar flares or man-made influences. Phase and Doppler frequency (i.e., the rate of change of phase) measurements on signals received from highly stabilized transmitters have become a standard technique for measuring

changes in the ionosphere. In the VLF band the phase changes measured are a few cycles over a day and therefore it is usually phase that is recorded. In the HF band phase, changes are typically thousands of cycles and Doppler frequencies are of the order of 1 Hz and therefore it is Doppler frequency that is usually recorded.

In the VLF band the conventional method of making measurements has been the use of some type of phase-tracking loop. This has the advantage of making extremely narrow noise bandwidths possible and permitting accurate tracking of very weak signals under high atmospheric noise level conditions. The concept of the system described here originated some two years ago and was proposed in the consideration of alternatives that might be employed to provide a digital output for automatic data processing from a VLF signal phase-tracking system. It was not implemented at the time in spite of its attractive features because of the high cost of available digital hardware. The recent remarkable drop in the cost of digital integrated circuits and the realization that the system could also provide high resolution Doppler frequency information in addition to phase, with a wide range of response times and scales suitable for use throughout the ionospherically propagated radio spectrum, prompted the construction of a prototype system.

2. BACKGROUND DISCUSSION

The conventional system for recording the phase of VLF and LF transmissions is the phase-tracking mechanical servo mechanism. Figure 1 shows a block diagram of a typical system. The output of the phase detector, which compares the signal phase with the reference phase after

passing through the phase shifter, drives the servomotor and phase shifter in a sense to keep the phase detector output at zero. If inertial effects are ignored, as shown in the anslysis in figure 1, this is a simple first-order feedback system, i.e., the velocity of the output is proportional to the system error and the phase shifter shaft follows the signal input phase changes with a simple exponential approach to equilibrium. The time constant can readily be controlled by the choice of the constant K, which is set by the mechanical gear ratio between the motor and phase shifter. In practice the inertia of the motor and other moving parts makes the system a second order one and necessitates the use of velocity feedback for stabilization.

The mechanical system is capable of excellent performance in the VLF signal-tracking application. Time constants suitable for the rates of change of phase encountered (10-100 s) are easily obtainable. Very low drift rates in the absence of signal are not difficult to achieve and maintain and this very much assists the maintenance of tracking under conditions where the signal is often interrupted. The mechanical system also has a perfect "memory" of its position during equipment power interruptions. It does not, however, have a natural digital output for use with automatic data processing systems, although encoders of various types can be added to the phase shifter. The mechanical part of the system is subject to wear and usually requires regular maintenance if the performance is not to become degraded.

It is natural that completely static solid-state systems should be sought as alternatives to the mechanical system for VLF phase measurements.

A number of commercial systems have appeared but the details of their design do not appear to have been published and none have provided digital data outputs or approached the flexibility of the system to be described. The basic electrical analog of the phase-tracking servomechanism is the phase-locked oscillator shown in figure 2. Here the frequency of a voltage-controlled oscillator (VCO) is proportional to the output of the phase detector, and a phase lock is maintained between the oscillator output and the input signal. As shown in figure 2 the response of the output, which measures the phase of the VCO with respect to the reference, is identical in form to that of the inertialess mechanical system of figure 1. The difficulty with this simple system is that of simultaneously obtaining adequate stability with the degree of voltage control required for a suitable range of response times. To obtain a no signal drift rate in the system of 1 cycle in 100 s, which is only marginal performance for a mechanical system, the VCO stability must be within .01 Hz. Among means to achieve this order of performance from the VCO are:

(a) The use of a voltage-controlled crystal oscillator. This approach has been successfully employed in one commercial VLF phase indicator, but it generally results in an inflexible system.

(b) The use of a higher frequency VCO than the signal frequency, and frequency division before comparison in the phase detector. This approach can yield useful results by virture of the freedom given the designer to choose the VCO operating frequency for the highest possible percentage stability.

(c) Mixing the VCO frequency with a stable reference frequency to

produce a sum frequency equal to the signal frequency. This gives the designer the freedom to choose the VCO frequency for maximum absolute stability, e.g., probably a much lower frequency than the signal.

All three techniques, singly or in combination, are valuable and can undoubtedly result in useful performance. The system described here can be regarded as the limiting case of (c), a block diagram of which is shown in figure 3. In this system, the VCO operates effectively at zero center frequency with positive and negative output frequencies corresponding to the bipolar input being indicated by mutually exclusive outputs on a pair of lines. The output is mixed with the 1-MHz reference frequency using a purely digital system that either adds or subtracts clock pulses fed to the subsequent divider system. The divider system is switched to accommodate signal inputs of either 1 kHz or 10 kHz, which correspond to the intermediate frequency outputs available from existing VLF/LF and HF receivers, respectively, in common use at ESSA Research Laboratories.

The first big advantage of this system is that it is easy to obtain drift rates comparable with the best mechanical systems. Operation of the VCO centered on zero frequency means that the stability of the slope of the voltage frequency characteristics becomes unimportant, and the absolute stability, which is enhanced by the subsequent division ratio, is extremely high.

The second advantage is that it becomes not only very simple to obtain a digital output representing phase but also one representing rate of change of phase (Doppler frequency). This is because the VCO

output now represents directly the difference between the signal and reference frequencies, so that direct integration in a bidirectional counter that is periodically reset gives the average offset, or Doppler frequency. Because of the division of the VCO-controlled frequency in the phase-tracking loop, the output counters operate in units of either 1/100 or 1/1000 or a cycle, thus giving excellent resolution.

3. DESCRIPTION OF THE PROTOTYPE SYSTEM (PHASE FREQUENCY DISPLAY)

3.1 General

The system has been mechanized in such a way that a complete assembly provides a great deal of flexibility and is suitable for making measurements over the whole ionospherically propagated radio spectrum. It can simultaneously provide visual numerical and analog outputs for local monitoring, in addition to digital outputs for automatic data processing. A separate digital output provides remote indication of housekeeping data, such as range settings, so that appropriate scaling can be carried through subsequent processing automatically. The system is divided into subassemblies in such a way that a user need buy no more facilities than are needed for his immediate application. A complete block diagram of the system is shown in figure 4 and photographs of the complete assembly together with examples of the largely integrated circuit subassemblies are shown in figure 5.

The minimum subunit complement giving a useful output is that contained above the dotted division in figure 4 labeled "basic loop", plus either the bidirectional phase or frequency counter and register. This

system gives a 10-bit digital output of the parameter selected and an analog signal amplitude output taken from the phase detector which is driven in phase with the signal. The remaining options, which can be added as desired, expand the digital outputs to include both phase and Doppler frequency and add analog outputs of phase and frequency derived through digital to analog converters, visual numerical displays of the digital outputs, a no signal lockout that can both indicate a drop in signal amplitude below a preset threshold and, if desired, disable the servo loop when this occurs, and a phase lock status indicator that indicates any occasion on which the phase lock error exceeds 90° and a cycle loss could have occurred.

The no signal lockout circuit has an additional input that enables external control of the lockout function, and the servo can be gated on and off in sympathy with the signal characteristics in systems, such as Omega, where this is appropriate.

Range switching enables the phase and Doppler frequency output scales to be varied over a wide range. The ranges provided are listed in tables 1 and 2, as part of the detailed specification given in the appendix. Notice that the most sensitive Doppler frequency ranges employ integration times of 100 s. This is not, however, inconsistent with the servo response times likely to be used on the VLF signals requiring such Doppler sensitivity. Table 3 lists the servo response times and tracking capabilities available.

Table 4 gives the location of the digital outputs. These are divided into two groups. The 24-bit group contains the 10-bit phase and 10-bit

Doppler frequency data together with the flag lines associated with signal amplitude, lockout status, and phase-lock status. The 12-bit group contains the housekeeping information on the phase and Doppler frequency scale multipliers and the servo response time.

3.2 System Description

The design of the major blocks in the system shown in figure 4 is treated in somewhat more detail in the following sections. In all cases, integrated circuits (IC) have been employed whenever practicable. All digital functions are realized by Diode Transistor Logic (DTL) nand gates, flip flops, and compatible units, such as monostable pulse generators.

3.2.1 Bidirectional Voltage-Controlled Oscillator

A block diagram of the VCO is shown in figure 6. The input voltage is applied to the operational amplifier and integrated in the capacitor C, which is selected by the servo response time switch. The integrator output is connected to two trigger circuits, one having a threshold at approximately +2.5 V and the other at -2.5 V. Both have a hysteresis of 2 V. When the integrator output reaches either threshold, the integrator is reset 2 V towards zero by the MOS transistor switch connected across the integration capacitor. For a fixed input voltage V, the circuit oscillates at a frequency f such that $f = \frac{V}{\Delta v\, RC}$, where Δv is the hysteresis of the trigger circuit.

The resistor R_2 is much larger than R_1 and serves to stabilize the d-c working point of the integrator and, in conjunction with the thresholds of the trigger circuits, to introduce a small dead zone of ± 3 mV input in which the VCO does not oscillate. This dead zone is similar in

effect to the break-away friction in a mechanical system and helps to prevent drift of the servo loop under no signal conditions. A typical voltage frequency characteristic is shown in figure 7.

Three outputs are provided by the VCO. The pulses on the add and subtract control line outputs are taken via buffers directly from the trigger circuit outputs and the pulse width is equal to the time required for the MOS transistor to reset the integrator. The clock pulse output is a constant 1-μs width pulse from the monostable circuit triggered by the back edge of both trigger circuit outputs. An additional input to the logic circuit (not shown) enables the MOS transistor switch to be held closed. This inhibits the VCO operation and enables the lockout functions to be implemented.

3.2.2 Add-Substract Control Circuit and Divider

The add and subtract control circuit takes the 1-MHz reference signal and provides an output for subsequent division whose average frequency is equal to 1 MHz plus or minus the VCO frequency. A block diagram is shown in figure 8. The timing of the VCO control pulses are first clocked to that of the 1-MHz square wave by the clocked JK flip flops. Two flip flops are used in a shift register configuration in each channel to eliminate spurious outputs due to simultaneous clock and VCO pulses. In the case of an add pulse input, a 250-ns pulse is generated by a monostable pulse generator and inserted into the square-wave output to form an extra pair of transitions. A subtract input generates a 1-μs pulse, which is used to suppress a pair of transitions. Both cases are illustrated in the waveforms in figure 8. The design of the VCO precludes

simultaneous add and subtract control pulses and limits the frequency of operation to $\simeq$ 10 kHz.

The output of the add-subtract control circuit is applied to counter circuits that are switched to divide by 50 or 500 to 20 kHz or 2 kHz, respectively, and then to a final pair of flip flops that are constrained to operate in quadrature and provide the drive to the phase detectors at either 10 or 1 kHz, depending on the signal input frequency in use.

3.2.3 Phase Detectors

Two detectors are used with the reference drives in phase quadrature. One detector drives the VCO, which maintains that reference in quadrature with the signal by virtue of the overall loop feedback. Thus the second detector is held in phase with the signal to provide signal amplitude information. In understanding the operation of the subsequent signal processing, it is important to realize that these detectors are essentially multiplicative mixers that take the signal spectrum and translate the carrier frequency to zero, i.e., d-c, with the noise sidebands folded over to extend from zero upwards. Thus, providing linearity can be maintained, the noise bandwidth can be limited to any desired extent by low pass filtering after the detector.

As far as the d-c output component is concerned, the phase detectors can be regarded as resolving two components in quadrature, i.e., for a signal phase ϕ_S and reference phase ϕ_R,

$$X \propto A \sin (\phi_S - \phi_R) \quad Y \propto A \cos (\phi_S - \phi_R),$$

where X and Y are the detector outputs and A is the signal peak amplitude.

Figure 9 shows a block diagram of the phase detectors. A common

input transformer provides a balanced output from an electrostatically screened bifilar secondary winding. The common point of the secondary is grounded and the antiphase outputs are switched alternatively into the output buffer amplifiers by MOS transistor switches. These are of the enhancement type and the use of a complementary pair enables a common bipolar (±12 V) drive signal to be employed, which is obtained from the 0-to +5-V reference input signal by an amplifier and level converter. The output buffer amplifiers provide some filtering of the a-c components of the detector output by means of a simple transitional RC network which provides some 30 dB of carrier filtering without introducing a critical extra phase shift in the pass band of the overall servo loop. In the case of the detector feeding the VCO, this network is switched to be appropriate for the carrier frequency in use.

The d-c stability of the phase detector used in the tracking loop is vital to maintaining a low drift rate under no signal condition. The normal operating signal level at the input to the buffer amplifiers corresponds to a phase-error sensitivity of 4.25 mV per degree. The buffer amplifiers have a gain of 10 and the VCO an operating threshold of $\simeq$ 3 mV so that the system can easily maintain a 1° tracking error for inputs 20 dB less than normal and a 10° tracking error for inputs 40 dB less than normal. This performance contributes greatly to the utility of the equipment under widely varying signal propagation conditions, but it does mean that a d-c stability of a few tens of microvolts referred to the input of the buffer amplifier is necessary if the VCO is to remain centered in its dead band under no signal conditions.

The amplifier design adopted to achieve this performance is somewhat of a compromise. It is necessary to minimize the bias current flowing back through the MOS transistor switches because this current becomes modulated at the reference frequency and the offset voltage developed at the amplifier input becomes dependent on the signal source impedance, which is not controlled. A similar problem arises as a result of unbalanced capacities in the MOS transistor switch circuits themselves, resulting in a net signal appearing across the input transformer and giving rise to an offset which is dependent on the source impedance and operating frequency. This can be adjusted to zero by providing resistive and capacitive balance adjustments on the phase detector feeding the VCO. To obtain the low bias current and d-c stability, a chopper-stabilized amplifier would have been desirable. Recently developed field-effect transistor (FET) input operational amplifiers, however, provide a performance that is almost equivalent without the complication and high price of the chopper type. The present design utilizes a well-matched dual junction FET source follower input to a standard 709-type integrated operational amplifier. This results in a temperature drift of about 10 μV/°C without any individual adjustment in the models so far constructed, which has proved satisfactory under laboratory environment conditions. For applications in other environments, where temperature changes greater than ±10°C are anticipated, it might be necessary to substitute a more expensive compensated FET or chopper-stabilized amplifier unit.

A carefully segregated ground system had to be used in the phase detector card to avoid coupling of coherent signals from other parts of

the system and to avoid the injection of spurious d-c chassis potentials into the output. A ground loop at the input is avoided by grounding only at the input coaxial connector at the rear of the unit. If problems are ever encountered because of a ground loop external to the unit, this ground can be removed with advantage. The circuit grounds associated with the level converters and power line decoupling are separated from those associated with the phase detector output. The former are taken to chassis ground adjacent to the phase detector card and the latter are carried across to a common single point ground at the VCO input.

Provision is made on the phase detector card for the signal amplitude output to be further filtered by connection of the front panel selected amplitude time constant capacitors to be connected across the amplitude buffer amplifier. This is only necessary if a no signal lockout card is not installed.

3.2.4 No Signal Lockout and Amplitude Measurement System

This is an optional card. If it is not installed, the amplitude output of the phase detector card is used directly, and as noted above the noise bandwidth is adjusted by connecting the capacitors used to select the amplitude time constant directly across the appropriate buffer amplifier.

As the term implies, the purpose of the no signal lockout is to sense the loss of a usable input signal and to lock up the phase servo loop so that the last recorded phase is retained until the signal reappears. This function can be of considerable value when recording intermittent signals. It is not satisfactory to rely completely on the

amplitude phase detector output because, if the signal happened to reappear in quadrature with the last recorded phase, there would be no d-c output to operate the signal threshold detector. Ideally both the quadrature components should be filtered to restrict their noise bandwidth equally and then combined to give the true amplitude independent of the signal phase by forming the rms sum $\sqrt{X^2 + Y^2}$. Although this can be done by analog methods it is relatively complicated and expensive. A simpler solution, which relieves the gross dependence of amplitude information on signal phase and is fully satisiactory for signal detection, is to form the sum $|X| + |Y|$, where $|X|$ and $|Y|$ are the magnitudes of X and Y irrespective of sign. This requires only full-wave rectification of the components, which can be achieved by standard operational amplifier techniques.

A block diagram of the system is shown in figure 10. Two IC amplifiers in unity gain configuration are used to filter the quadrature components through a single RC time constant that is selectable at the front panel as 0.1, 1.0, or 10 s. After passing through these filters, the signals are applied to the two full-wave rectifier circuits, which employ a further pair of IC amplifiers with diode feedback to achieve linear rectification over a wide dynamic range. The outputs are then summed in two separate unity gain IC amplifiers. One amplifier supplies the external amplitude output. The second, which has a fixed 10-s time constant filter, feeds the signal level threshold detector. This detector uses a 710-type IC comparator with feedback to provide a hysteresis of $\simeq$ 150 mV and a signal acquisition threshold adjustable from +150 mV to

+2.5 V by means of a preset control.

The output of the threshold detector is applied to a logic gate system that provides the following outputs:

(a) a front panel lamp and external flag line indicating that no signal is present, and

(b) an "enable" output that controls the VCO operation. The VCO is disabled if there is no signal and the front panel lockout control switch is on, or if the external enable input logic level is zero. A "wired or" connection in parallel with this output enables the VCO to also be controlled by the register transfer circuits.

3.2.5 Bidirectional Counters

The basic bidirectional counter used throughout the system is shown in figure 11. This is a simple clocked binary counter. The counting direction reversal is achieved by selecting the complement of the required condition for carry from one stage to the next. The change-over operation is carried out on each counter by four gates connected as an RS flip flop, which is fed by the add and subtract control pulses from the VCO and serves both to reduce the loading on these pulse lines and to store the required direction of counting. The change-of-direction control occurs at the front edge of the control pulses and thus allows plenty of time before the clock pulse, which is generated at the back edge of the control pulses. Each octal group reforms the clock pulse according to the carry condition from that group. In addition, the range-selection dividers that set the scale factors of the main phase and

frequer y counters have clock outputs at division ratios of 2 and 4 as well as The main counters consist of two octal groups plus a third group in which the output clock buffer is replaced by a further flip flop to give a total resolution of 2^{10} (1024).

3.2.6 Output Register and Control System

Output registers of the IC parallel transfer type are used on both the phase and frequency counters. Transfers are initiated by the reset and transfer control system. An external clock pulse at 1 pps is required to time this operation. To prevent errors that may result from carrying out a transfer while a carry is propagating in the counter, the VCO is disabled for 10 μs. After the 2 μs allowed for completion of any count in progress, the register transfer on the frequency counter is made. A further 2 μs is allowed before any reset operation is initiated. Only the frequency counter is reset and this to midscale (1000 octal). To obtain the reset repetition rate, the 1-pps input is divided down to 1/10 and 1/100 pps and the appropriate value selected depending on the integration time required. The phase counter register transfer is made once per second at the end of the 10-μs period during which the VCO is disabled.

The external digital outputs are fed via standard DTL gates used as buffers to prevent any external short circuits or signal pickup from affecting the operation of the registers.

3.2.7 Output Displays and Analog Outputs

Two types of output display can be provided. The first is a simple 10-lamp system displaying the state of each 10-line binary output; the

second is a cold cathode tube type of visual numerical display. To simplify the decoding required, the display is in octal base numbers. The case of the phase display is straightforward, but in the case of the frequency display it is necessary, for convenient interpretation, to take into account that zero frequency is represented by midscale on the counter (1000 octal) and positive and negative excursions are represented by increases and decreases about this value. Although this is perfectly convenient for subsequent automatic data processing, it is more natural to display a true zero and positive and negative excursions about zero. This is achieved in the numerical display decoder quite simply by interpreting the most significant bit as a sign bit and causing the presence of a zero, indicating a negative number, to substitute the ones complement value into the octal decoder. The result is two values of zero, one positive and one negative, and a display error of 1 count for negative numbers. The complication of arranging for an end-around carry in the decoder was not considered worthwhile to correct an error that only affects the display and not the main digital output.

Provision is made for two commercial digital-to-analog converters to be fitted where analog outputs of phase and offset frequency would be desirable. These are 10-bit converters with 0.1-percent accuracy that are available in module form. The converter used for the phase output gives 0 to +5 V : ll scale; one for the frequency output is offset to bring zero frequency to zero output and has a range of +2.5 V to -2.5 V.

3.2.8 Phase Lock Status Indicator

This is an option that can be added to provide both a digital flag

output and a front panel warning when the servo tracking error exceeds 90° and a cycle loss could have occurred. The condition is sensed by checking the amplitude phase detector output for a negative voltage. The phase detector output is first filtered by an active filter providing 12 dB per octave attenuation above 50 Hz and is then applied to a threshold trigger circuit operating at ≃ -100 mV and having a 100-mV hysteresis. If the trigger circuit senses a voltage in excess of -100 mV, a flip flop is set and, through a clocked shift system, a second flip flop is maintained set for the complete 1-s period (timed by the 1-pps input) immediately following the alarm. This system ensures that the digital flag output exists for a minimum of 1 s so that it can be transferred to other equipment. The flag line logic cancels the phase lock loss indication if a no signal condition also exists.

The phase lock status indication must be interpreted with care because large noise signals are capable of producing a perfectly genuine loss of lock, which, however, is quite unimportant.

4. RESULTS

The general performance of the prototype unit has been fully up to theoretical expectations and the preliminary experimental results indicate that the system should be a valuable addition to the available techniques for phase and Doppler frequency measurements of ionospherically propagated radio signals. Some examples of chart records made using the analog outputs of the system are given in figures 12 through 15.

Figure 12 shows a Doppler frequency recording made with the digital system placed side by side with a spectral analysis of the same signal. Although the digital system (upper record) cannot, of course, display

different frequency components arriving simultaneously, it is often able to suggest their simultaneous presence by switching between them as one or the other becomes dominant. A good example of this behavior occurs between 1230 and 1235 UT in figure 12. The relative advantages of different Doppler frequency display techniques has been covered elsewhere (Grubb, 1968).

Figure 13 shows a phase track record for an 8.9-MHz signal propagating 24 hr over a 1200 km-path. The apparent repeatability of this record is somewhat surprising and will be the subject of further investigation.

Figure 14 shows a VLF phase and Doppler frequency record of the NPM, 23.4-kHz transmission received at Boulder, Colorado. This is a comparatively strong noise-free signal, showing strong modal interference effects over the sunrise and sunset periods (around 1400 and 0300 UT) that cause the total diurnal phase shift to be non-zero. The Doppler frequency record clearly shows these interference effects and demonstrates that this output could readily be used for the automatic recognition of solar flare effects, which have similar onset rates. The small discontinuities in these records, for instance at around 1000 UT, are caused by switches in transmitter modulation from on-off keying to frequency shift keying, which apparently result in temporary transmitted phase discontinuities.

Figure 15 shows a similar VLF phase and Doppler frequency record made with the same servo response time (10 s) but this time of the GBR, Rugby, England, 16-kHz transmission received at Boulder, Colorado. This is a weaker signal as reflected in the signal-to-noise ratio of the

records. The phase record is regular and trapezoidal in form as would be expected for simple propagation on an east-west path of this length. The Doppler record shows a relatively constant noise fluctuation of about 0.5-mHz peak-to-peak amplitude and it should still be possible to automatically recognize events exceeding 1 mHz in Doppler frequency, particularly if this rate persists for several sample periods.

5. CONCLUSION

An instrumentation concept and its practical realization are described that should contribute considerably towards digital data acquisition systems for radio wave experiments as well as making possible real-time Doppler frequency measurements of the dominant signal component with much greater sensitivity and stability than previously available.

6. ACKNOWLEDGMENTS

The concept of this equipment originated during work carried out by the author while employed by the United Kingdom Atomic Energy Authority. The credit for construction of the prototype and for much of the experimental work belongs to Mr. Carl Holmes of the Space Disturbances Laboratory, ESSA, who was responsible for the mechanical design and many useful improvements to the electrical design.

The work described was funded by the Advanced Research Projects Agency of the Department of Defense under Order Number 932.

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APPENDIX

Specification of the Digital Phase Servo Unit

1. Signal input.

   One kHz or 10 kHz selected by a front panel switch

   Input impedance: 1 KΩ

   Nominal input level: ≃ 250 mV rms

   Maximum coherent input level: 1 V rms

   Minimum input level: 2.5-mV rms results in a phase tracking dead zone of ≃ 10°

   Maximum noncoherent input level: 5-V peak

2. Reference input: 1 MHz

   Input impedance: 1 KΩ

   Minimum input: 1 V pk-pk

3. Timing input: 1 pps, 0-to +5-V logic levels. Operation on the positive or negative going transition can be selected internal linking.

4. Cumulative phase output.

   (a) Digital 10-bit binary. Levels, 0 < 0.5 V, 1 > 4 V from 6 KΩ source. Signal phase advance indicated by increasing number. Output static for 1 s. Change occurs ≃ 10 μs after 1-pps timing edge transition.

   (b) Optional analog 0 to +5 V; output goes positive for advancing phase. Output impedance < 2 Ω. Maximum output current ±10 mA.

   (c) Optional visual display.

   Ten-lamp binary or numerical display 0-1777 octal base.

Ranges are front panel switch selected. See table 1.

5. Offset frequency output.

(a) Digital 10-bit binary. Levels (0 > 0.5 V, 1 > 4 V from 6 KΩ). Output static for 1, 10, or 100 s depending on range selected. Change occurs ≃ 2 μs after 1-pps timing edge transition. Zero frequency is offset to 1000 octal; +1 = 1001 octal, -1 = 0777 octal.

(b) Optional analog output.

Plus or minus 2.5 V about zero. Output impedance < 2 Ω. Maximum current ± 10 mA.

(c) Optional Display.

Ten-lamp binary or numerical ± 777 octal.

Ranges are front panel switch selected. See table 2.

6. Response times.

Front panel switch selected. See table 3.

7. Amplitude output.

Front panel selected time constants of 0.1, 1.0, and 10 s. Output 0 to 5 V. Output impedance < 2 Ω. Maximum current ± 10 mA. Output for nominal signal input ≃ 2.5 V. Front panel meter displays 0 - 5V. Optional no signal lockout circuit provides a threshold indication on a digital flag output, a front panel lamp indicator and, if selected by a front panel switch, disables the servo when the signal level is below threshold. Switch position indicated by additional flag output. Threshold for signal acquisition adjustable by internal preset control from ≃ 15-mV to 250-mV rms signal input. Hysteresis ≃ 15 mV rms.

8. Phase lock status indicator.

   Optional unit provides a digital flag output and front panel lamp indicator if the servo loop error exceeds 90° and a cycle loss is likely to occur. Output present for 1-s minimum.

9. Digital housekeeping data.

   Twelve-line digital output; 0 indicated by short to ground; 1 by +5 V through 1 KΩ. Indicates settings of phase and frequency range multiplier switches and the servo response time switch. Coding given in tables 1, 2, and 3, respectively.

10. External enable input.

    This is used to externally control the servo loop operation. Logic level; 1 allows the servo to operate; 0 disables the servo. If the input is not used it should be left open circuit.

11. Digital output locations. See table 4.

Table 1. Phase Span (0-1024) Multipliers and Total Spans

Panel switch position	Output code (octal)	1-kHz Input		10-kHz Input	
		Multiplier all $x10^{-3}$	Span (cycles)	Multiplier all $x10^{-2}$	Span (cycles)
1	0	1	1.024	1	10.24
2	1	2	2.048	2	20.48
3	2	4	4.096	4	40.96
4	3	8	8.192	8	81.92
5	4	16	16.38	16	163.8
6	5	32	32.77	32	327.7
7	6	64	65.54	64	655.4
8	7	128	131.1	128	1311
9	10	256	262.1	256	2621
10	11	512	524.3	512	5243

Table 2. Doppler Frequency (±512) Multipliers and Spans

Panel switch	Output code (octal)	Integration time (seconds)	1-kHz Input		10-kHz Input	
			Multiplier	Approx. span (Hz)	Multiplier	Approx. span (Hz)
1	0	1	8×10^{-3}	±4	8×10^{-2}	±40
2	1	1	4×10^{-3}	±2	4×10^{-2}	±20
3	2	1	2×10^{-3}	±1	2×10^{-2}	±10
4	3	1	10^{-3}	±0.5	10^{-2}	±5
5	4	10	4×10^{-4}	±0.2	4×10^{-3}	±2
6	5	10	2×10^{-4}	±0.1	2×10^{-3}	±1
7	6	10	1×10^{-4}	±0.05	1×10^{-3}	±0.5
8	7	100	4×10^{-5}	±0.02	4×10^{-4}	±0.2
9	10	100	2×10^{-5}	±0.01	2×10^{-4}	±0.1
10	11	100	1×10^{-5}	±0.005	1×10^{-4}	±0.05

Table 3. Response Times and Approximate-Tracking Rate Capabilities

Tracking rate switch position	Output code (octal)	1-kHz Input		10-kHz Input	
		Response time (seconds)	Tracking rate (Hz)	Response time (seconds)	Tracking rate (Hz)
1	0	1000	0.001	100	0.01
2	1	330	0.0033	33	0.033
3	2	100	0.01	10	0.1
4	3	33	0.033	3.3	0.33
5	4	10	0.1	1	1
6	5	3.3	0.33	0.33*	3.3
7	6	1	1	0.1*	10
8	7	0.33*	3.3	0.033*	33
9	10	0.1*	10	0.01*	100
10	11	*	20*	*	200*
11	12	*	50*	*	500*

*Response times influenced by carrier filtering and output data systems.

NOTE: The response of the phase-tracking loop to a small step change in phase $\Delta\varphi$ at t=0 is exponential and of the form $\varphi(t) = \varphi(0) + \Delta\varphi(1-e^{-t}/T)$. The response time quoted is T, the time required to reach 63 percent of the final value. The tracking-rate capability is arbitrarily defined for a phase-tracking error of $\simeq 0.6$ rad. Both quantities are proportional to the input amplitude and are quoted for nominal input (midscale on panel meter, 2.5-V output on the amplitude line).

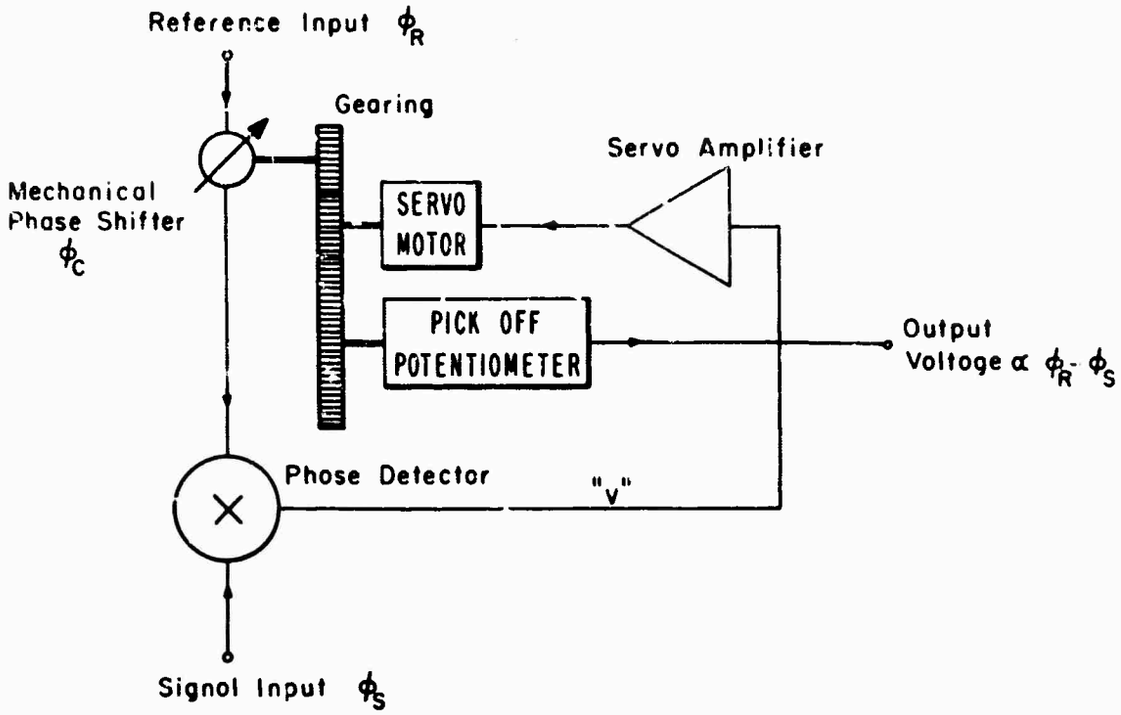
Table 4. Digital Outputs

Socket 1

Information		Pin	Notes
Digital phase 10-bit binary	LSB	A	Information updated each second on the second; 0-1777 octal.
		B	
		C	
		D	
		E	Signal phase advance indicated by increasing number.
		F	
		H	
		J	
		K	
	MSB	L	
Digital frequency 10-bit binary	LSB	a	Information updated each second on the second.
		b	
		c	
		d	
		e	Midscale zero frequency = 1000 octal.
		f	
		h	
		j	Positive frequency offset indicated by increasing number.
		k	
	MSB	m	
No signal flag		M	High when no signal threshold crossed.
Lockout status		p	High when lockout disabled.
1-kHz/10-kHz input		n	High for 1-kHz operation.
Phase lock status		r	High for 1-s minimum if phase lock lost.
Ground		N	

Socket 2

4-bit binary Phase multiplier Switch position	LSB	A	Housekeeping information. For subsequent processing.
		B	
		C	
	MSB	D	
4-bit binary Frequency multiplier Switch position	LSB	E	
		F	
		H	
	MSB	J	
4-bit binary	LSB	K	
		L	
Servo response time		M	
	MSB	N	
Ground		P	



Overall Constant of Amplifier/Motor/Phase Shifter = K_1 Radians sec^{-1} $Volts^{-1}$

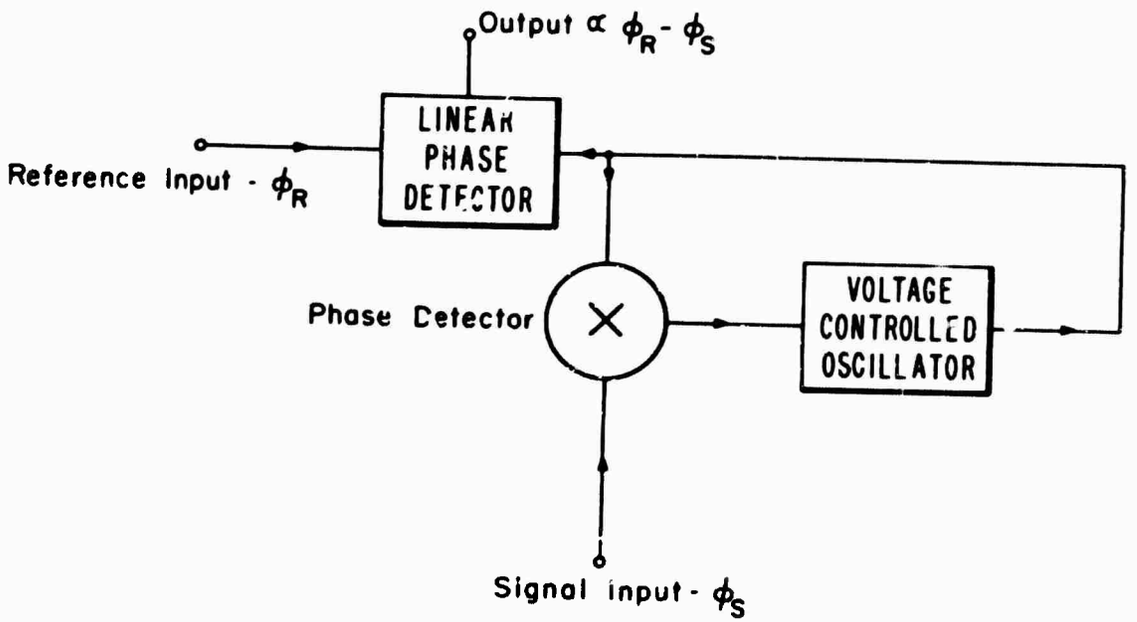
Phase Detector Constant = K_2 Volts $Radians^{-1}$

$$\Delta\phi = K_1 \int v\, dt \qquad v = K_2(\phi_R + \phi_C - \phi_S)$$

Solution for a Step Change in $\phi_S = \Delta\phi$ at $t = 0$

$$(\phi_R + \phi_C)_t = (\phi_R + \phi_C)_0 + \Delta\phi(1 - e^{-t/T}) \qquad T = 1/K_1K_L$$

FIG. 1 MECHAN.CAL PHASE-TRACKING SERVOMECHANISM SYSTEM



VCO Constant = K_1 Radians sec^{-1} $Volt^{-1}$

Phase Detector Constant = K_2 Volts $Radians^{-1}$

Response Time Constant = $\frac{1}{K_1 K_2}$

FIG. 2 SIMPLE PHASE-LOCKED OSCILLATOR USED AS A PHASE MEASUREMENT SYSTEM

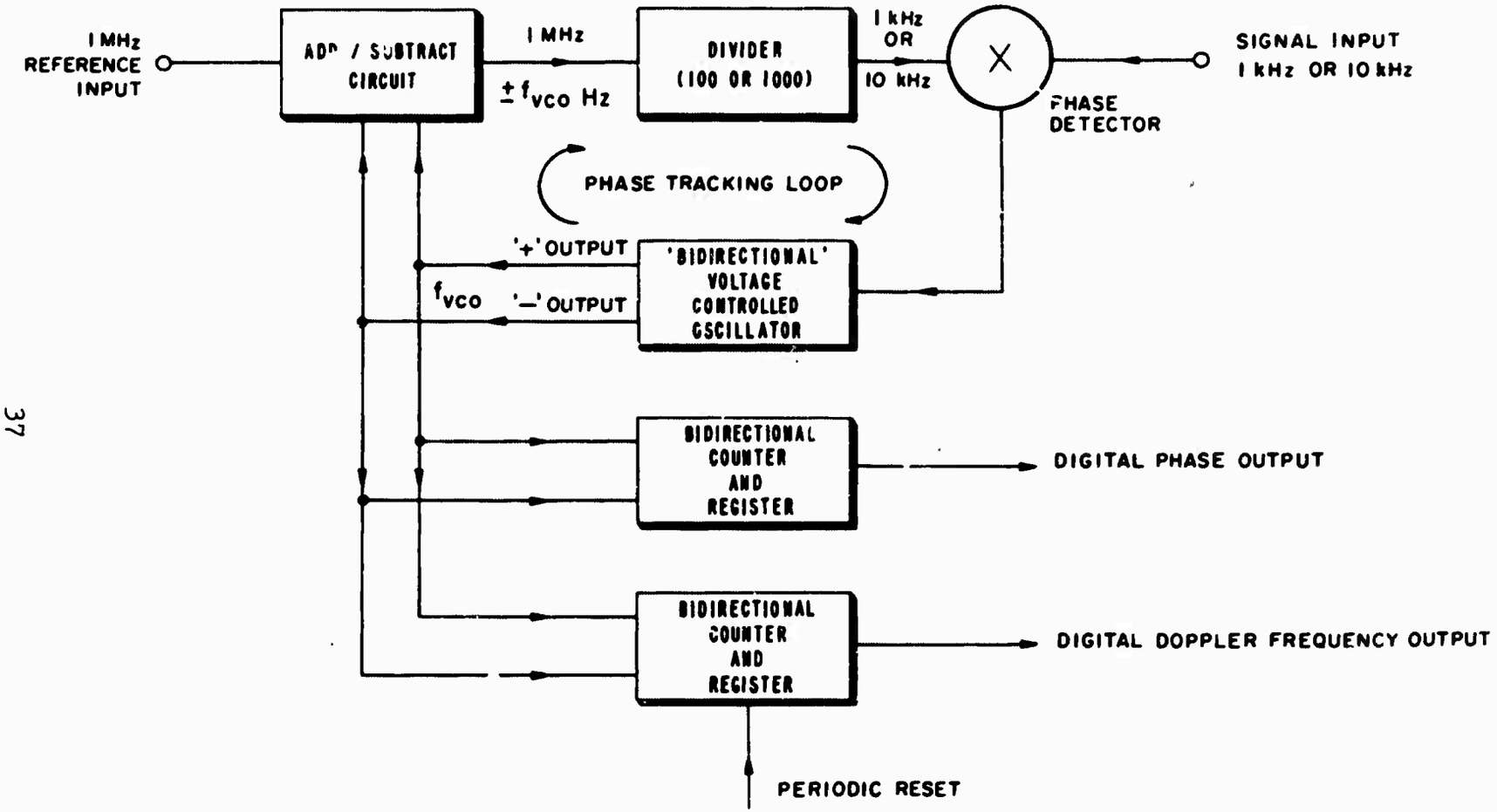


FIG. 3 BLOCK DIAGRAM OF A DIGITAL PHASE-TRACKING LOOP WITH A DOPPLER FREQUENCY OUTPUT

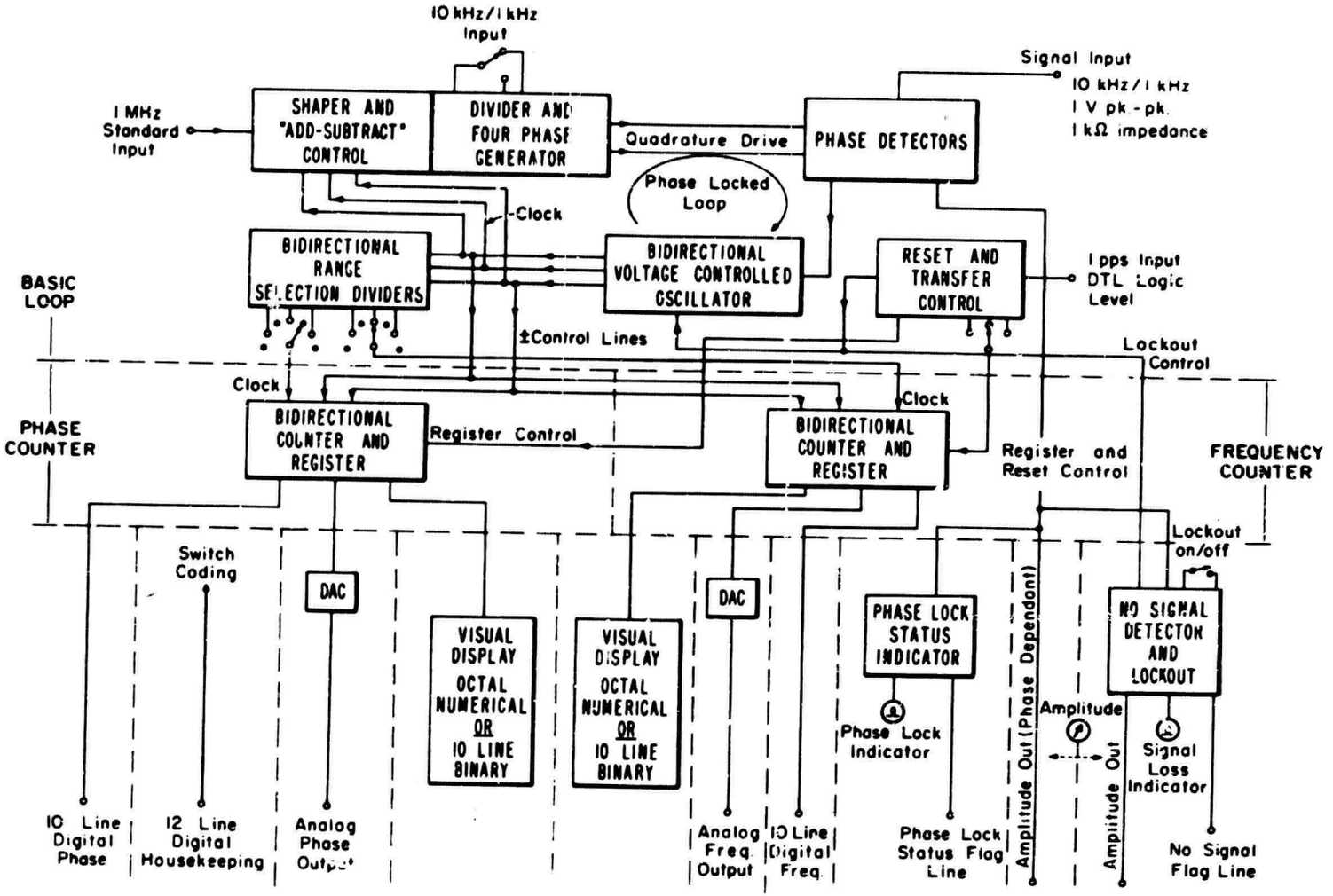


FIG. 4 BLOCK DIAGRAM OF THE DIGITAL PHASE SERVO UNIT

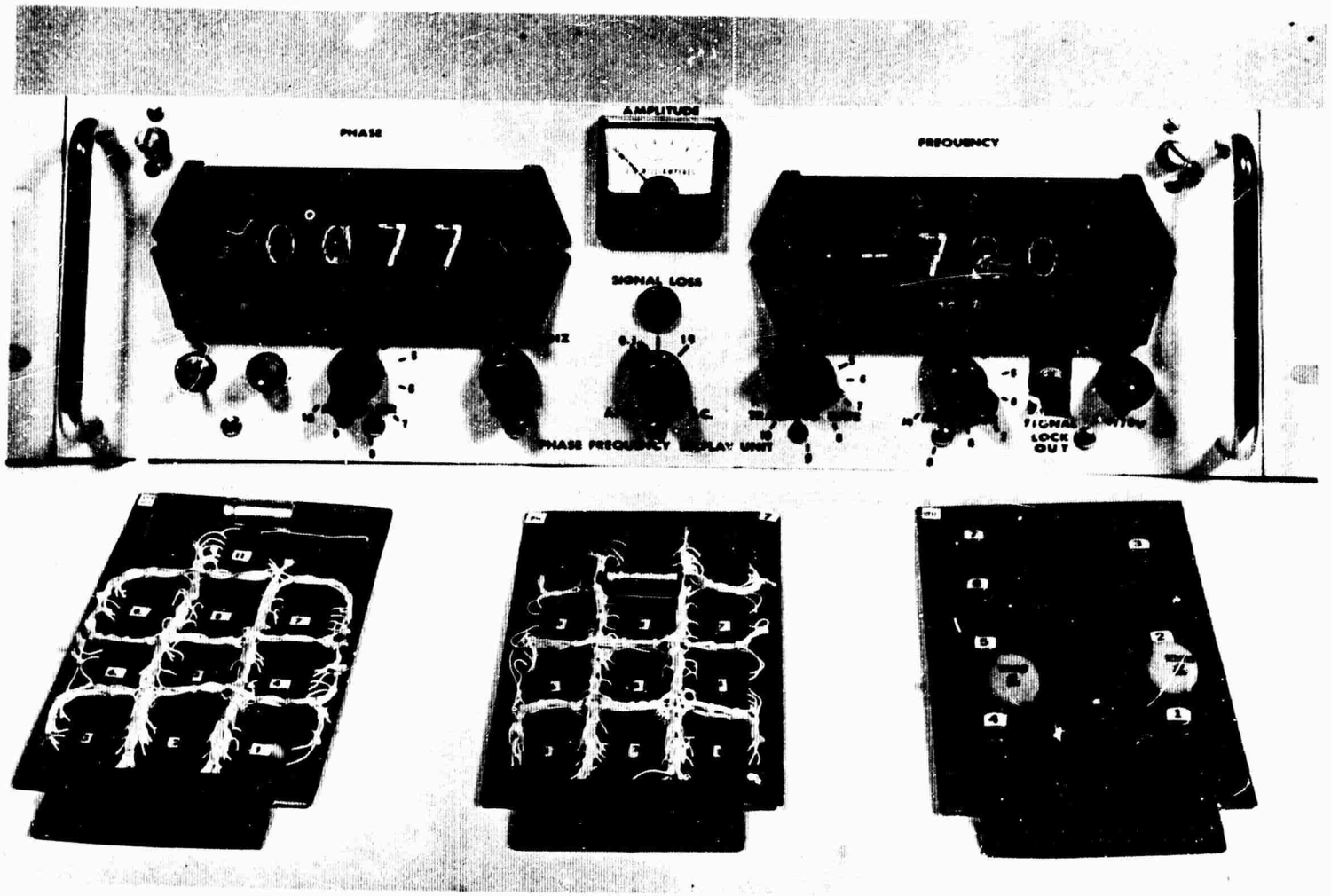


Fig. 5 Front Panel View of the Digital Phase Servo Unit

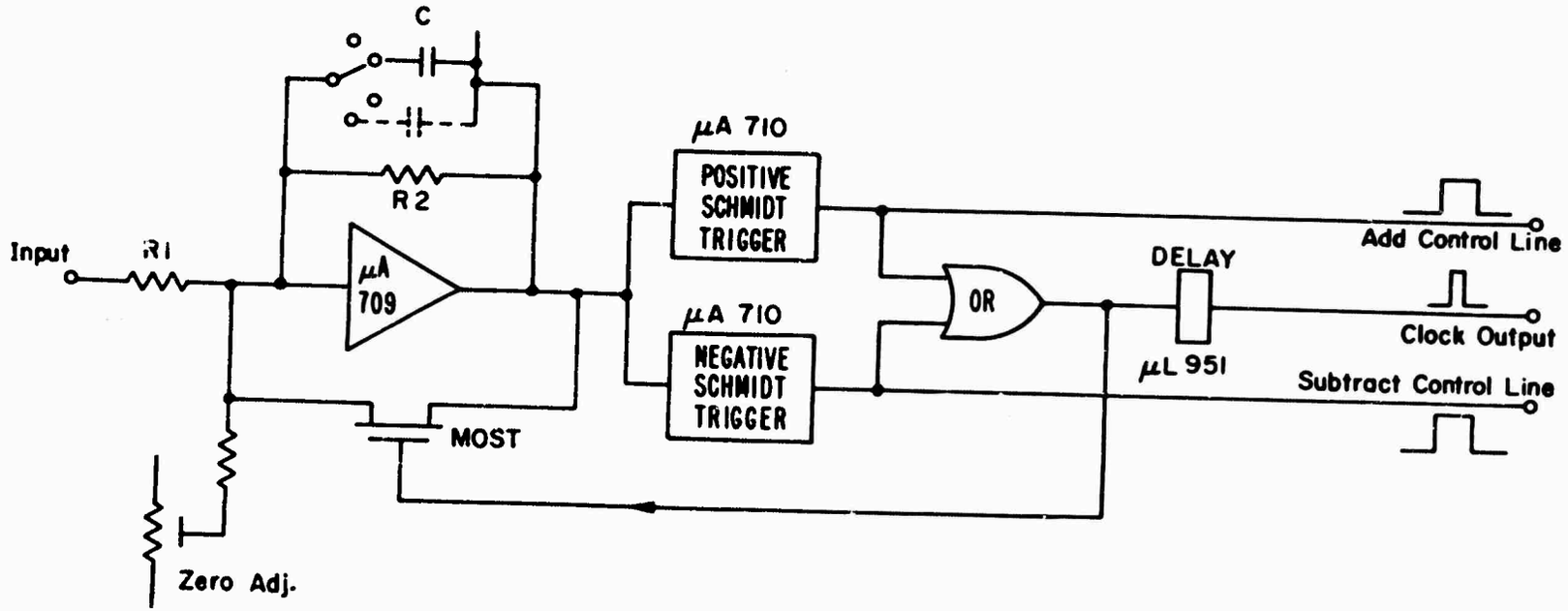


FIG. 6 BLOCK DIAGRAM OF THE BIDIRECTIONAL VOLTAGE-CONTROLLED OSCILLATOR

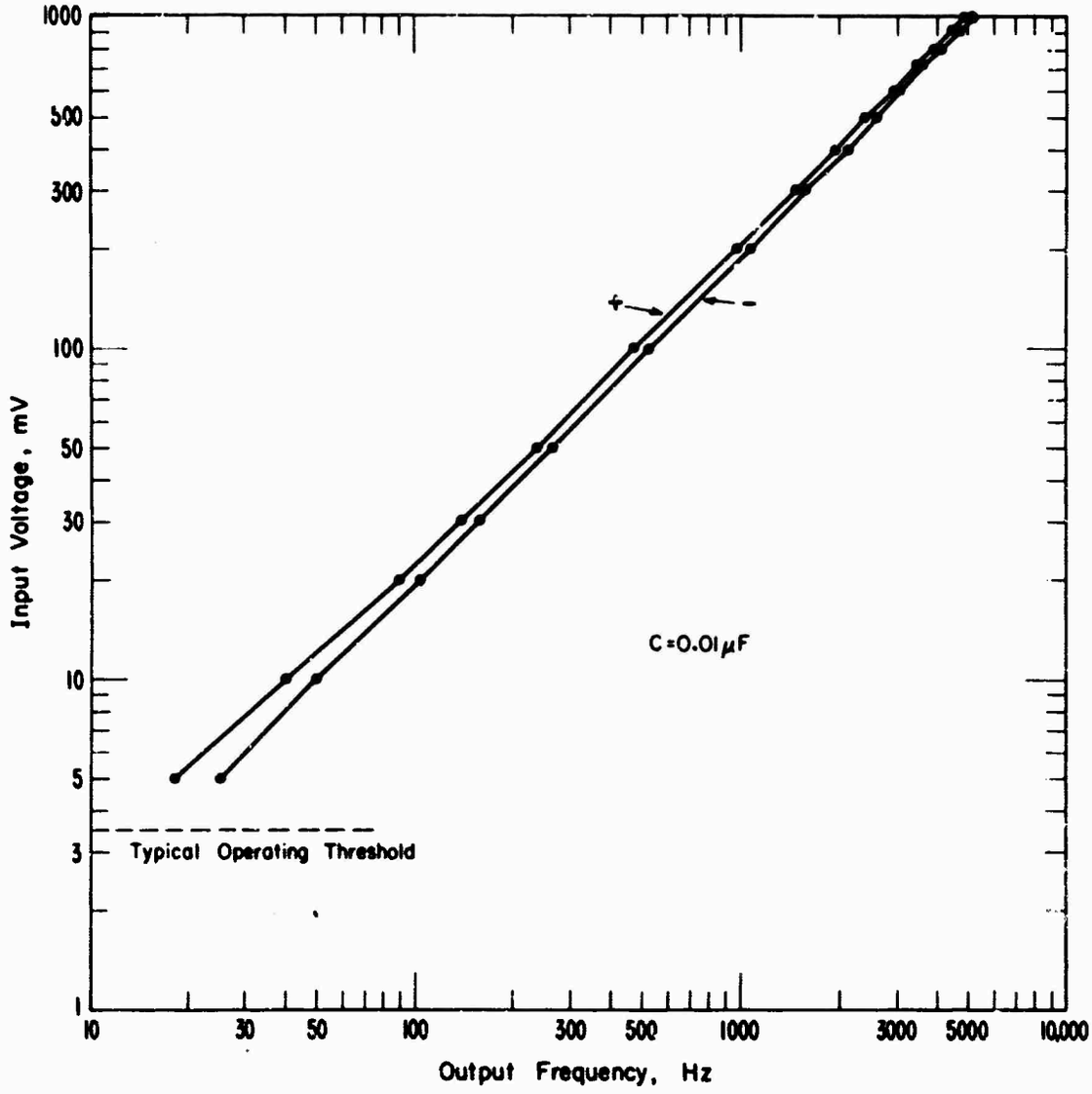


FIG. 7 TYPICAL BIDIRECTIONAL VOLTAGE-CONTROLLED OSCILLATOR CHARACTERISTIC

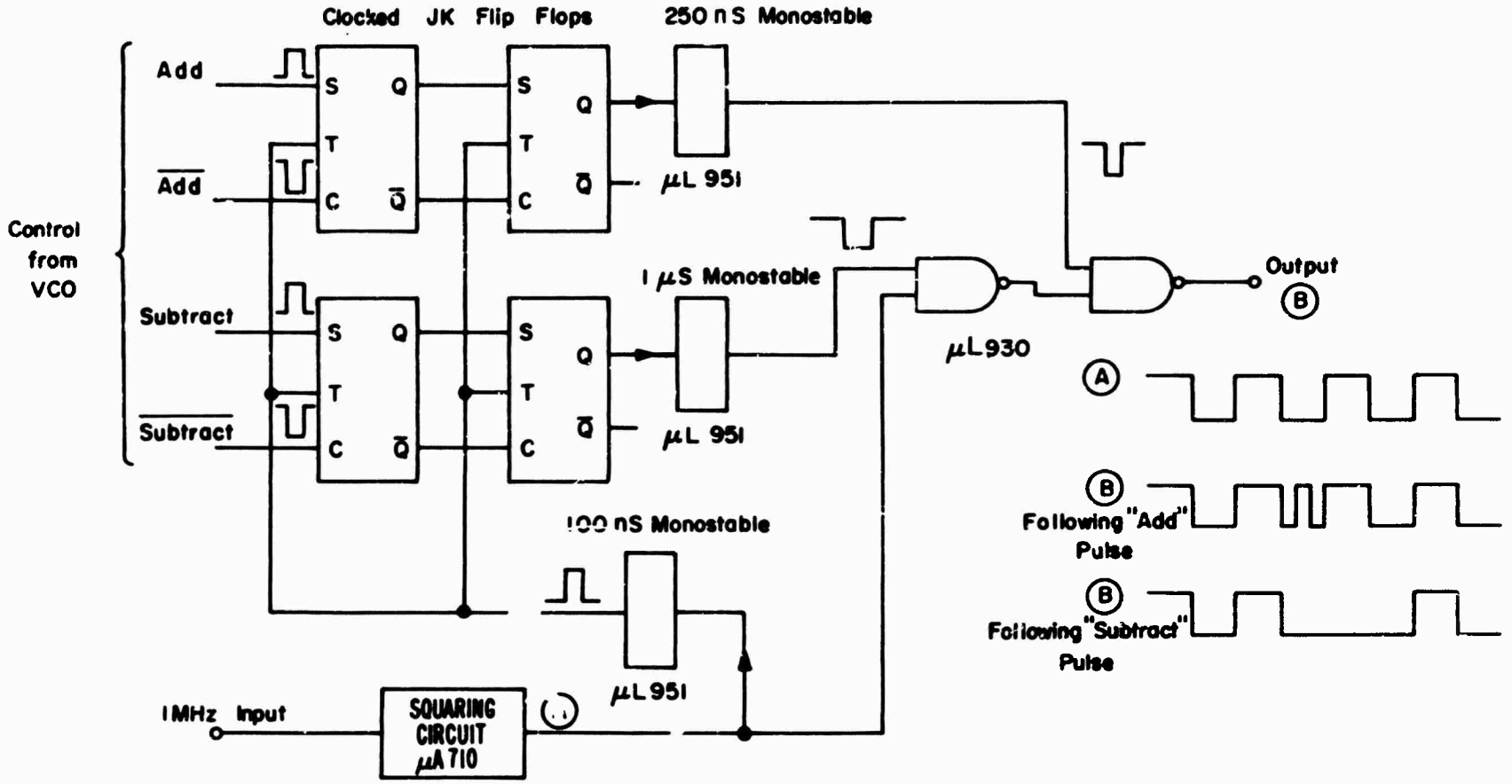


FIG. 8 BLOCK DIAGRAM OF ADD SUBTRACT CONTROL CIRCUIT

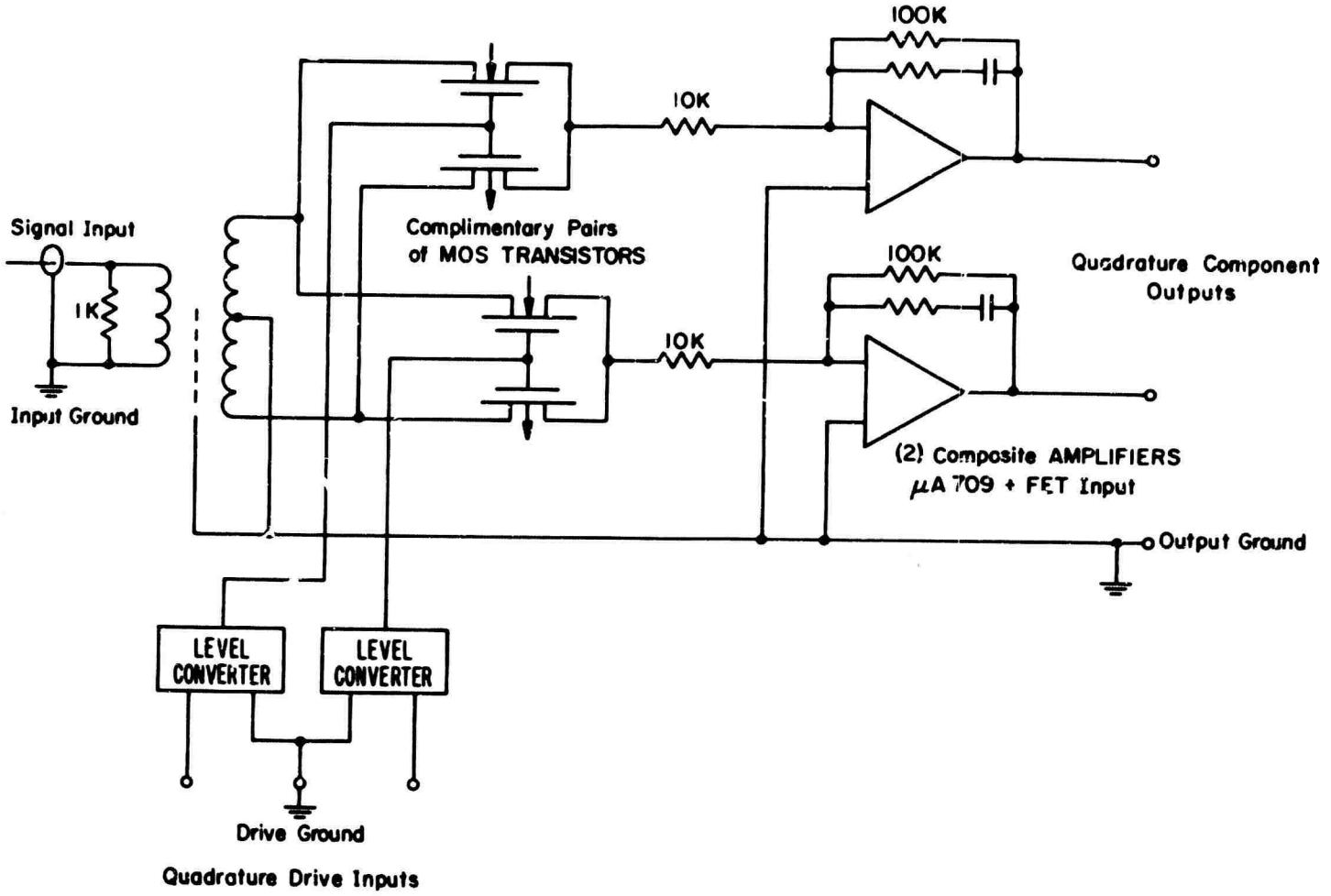


FIG. 9 BLOCK DIAGRAM OF THE PHASE DETECTORS

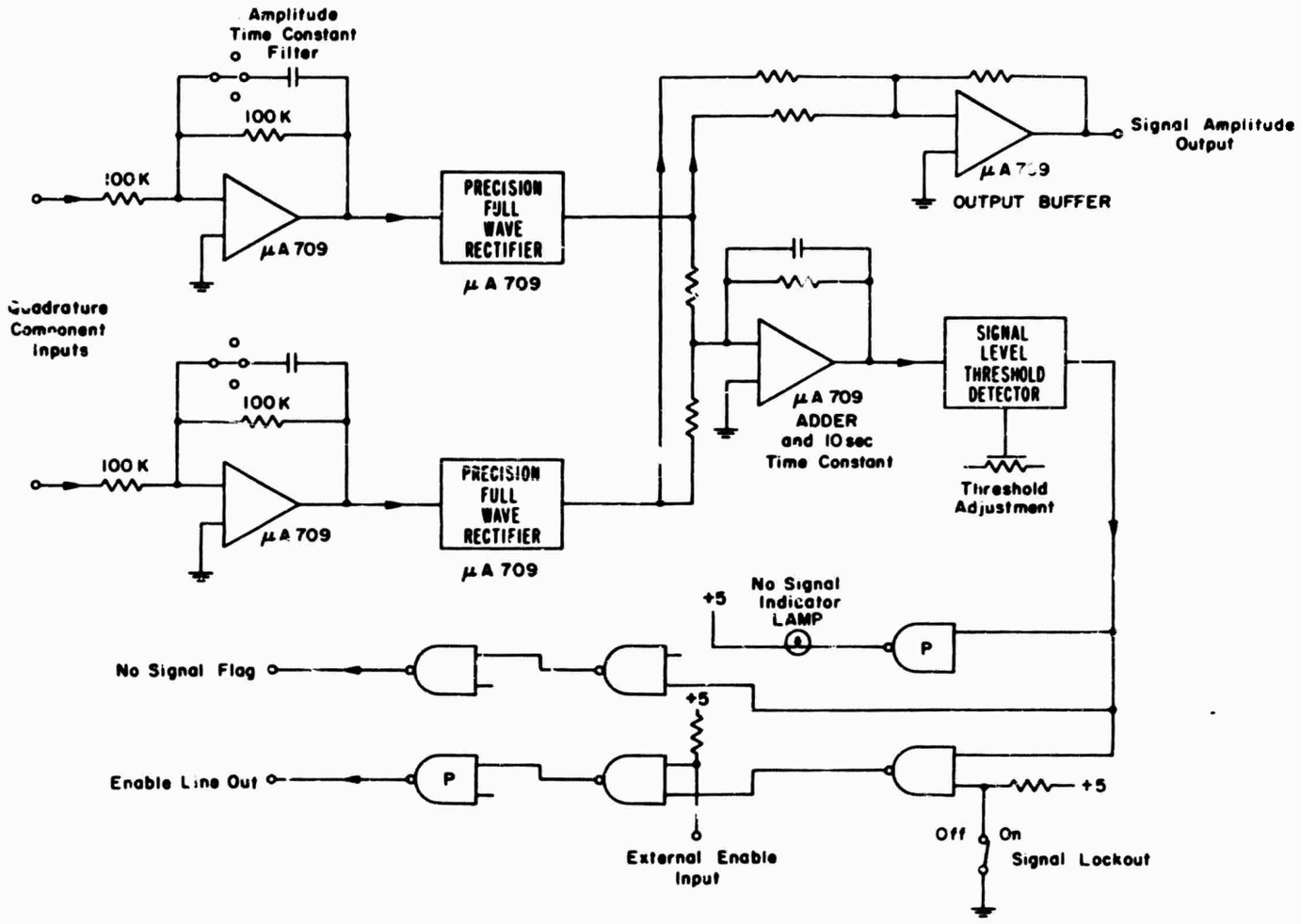


FIG. 10 BLOCK DIAGRAM OF NO SIGNAL LOCKOUT
AND AMPLITUDE MEASURMENT

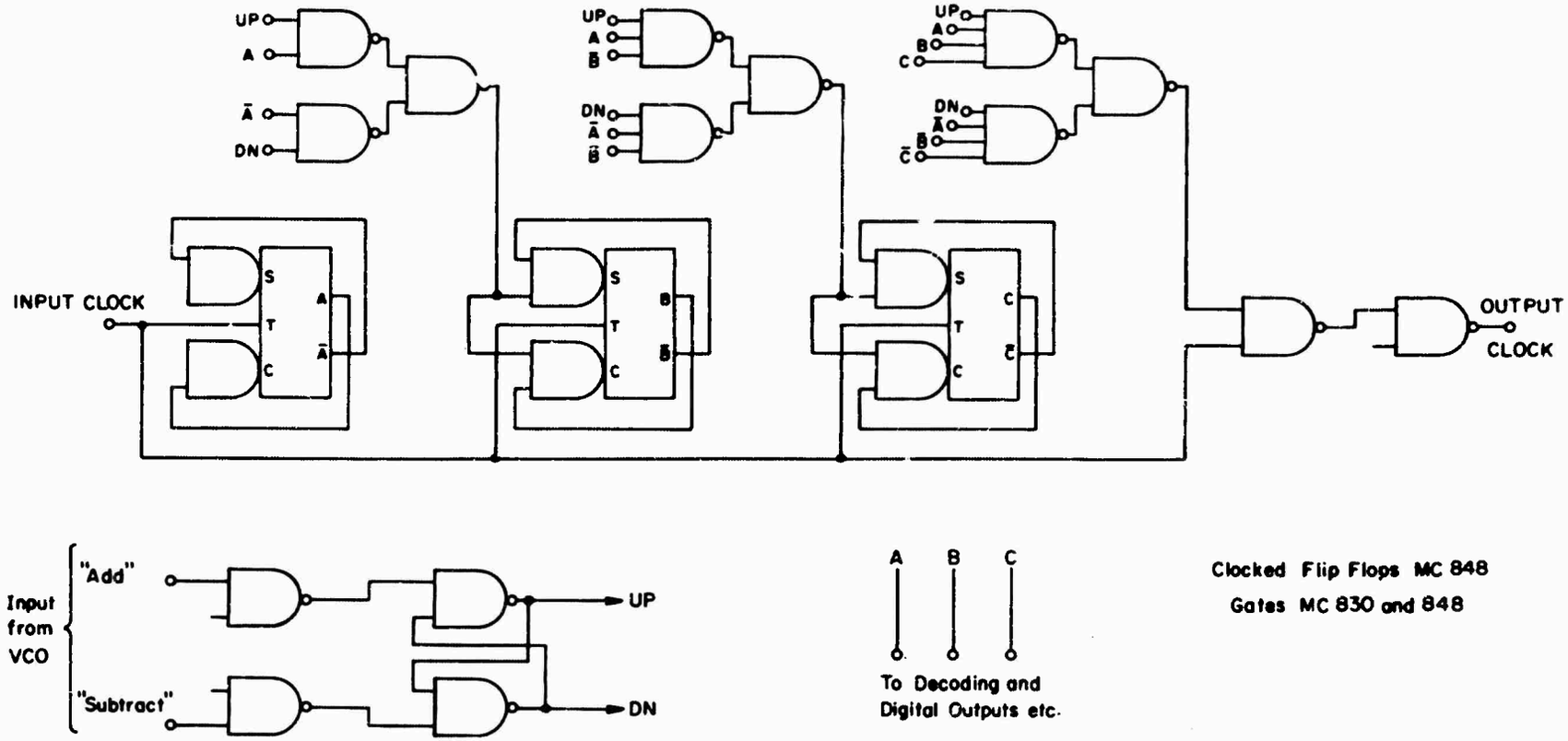


FIG. 11 BLOCK DIAGRAM OF BASIC OCTAL BIDIRECTIONAL COUNTER

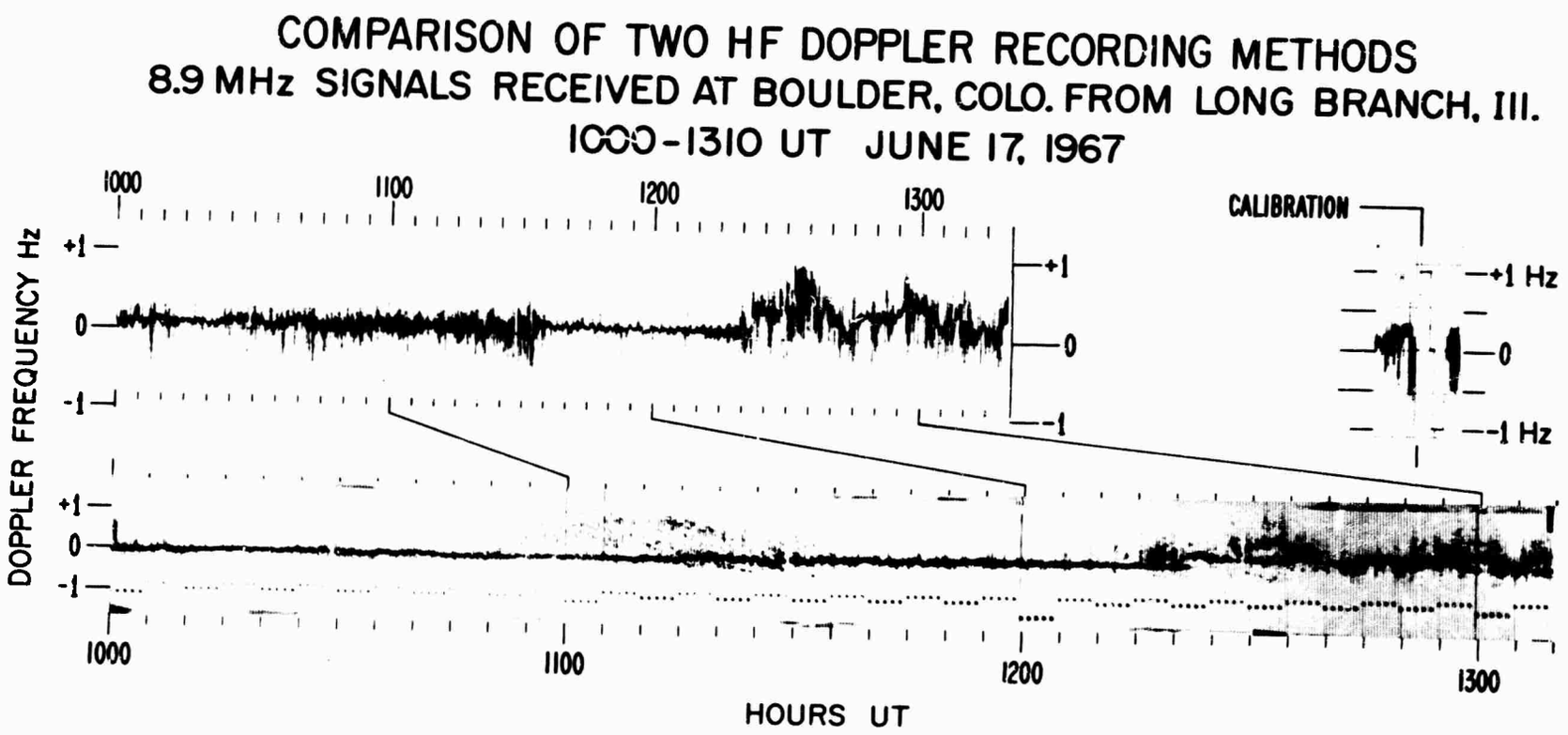
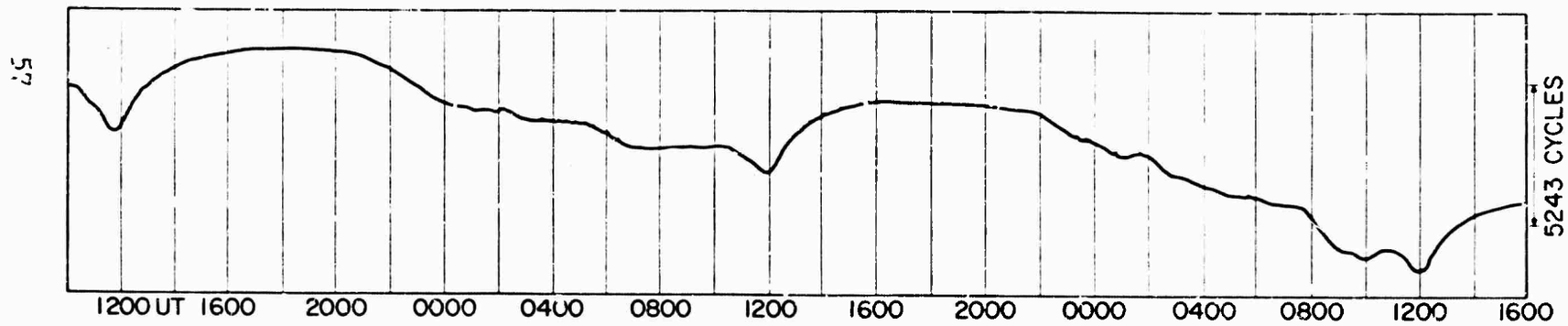

COMPARISON OF TWO HF DOPPLER RECORDING METHODS
8.9 MHz SIGNALS RECEIVED AT BOULDER, COLO. FROM LONG BRANCH, III.
1000-1310 UT JUNE 17, 1967
1000
1100
1200
1300
CALIBRATION
+1 Hz
0
-1 Hz
+1
0
-1
DOPPLER FREQUENCY Hz
HOURS UT

Fig. 12

EXAMPLE OF HF PHASE-TRACKING RECORD TAKEN WITH THE DIGITAL PHASE SERVO UNIT

8.9 MHz FROM HAVANA, ILLINOIS RECEIVED AT BOULDER, COLORADO
OCTOBER 24-26, 1967



PHASE (RESPONSE TIME 100 ms)

Fig. 13

EXAMPLE OF PHASE AND DOPPLER FREQUENCY RECORDS FROM THE DIGITAL PHASE SERVC UNIT

NPM Hawaii to Boulder, Colo. 23.4 kHz Oct 12-13 1967

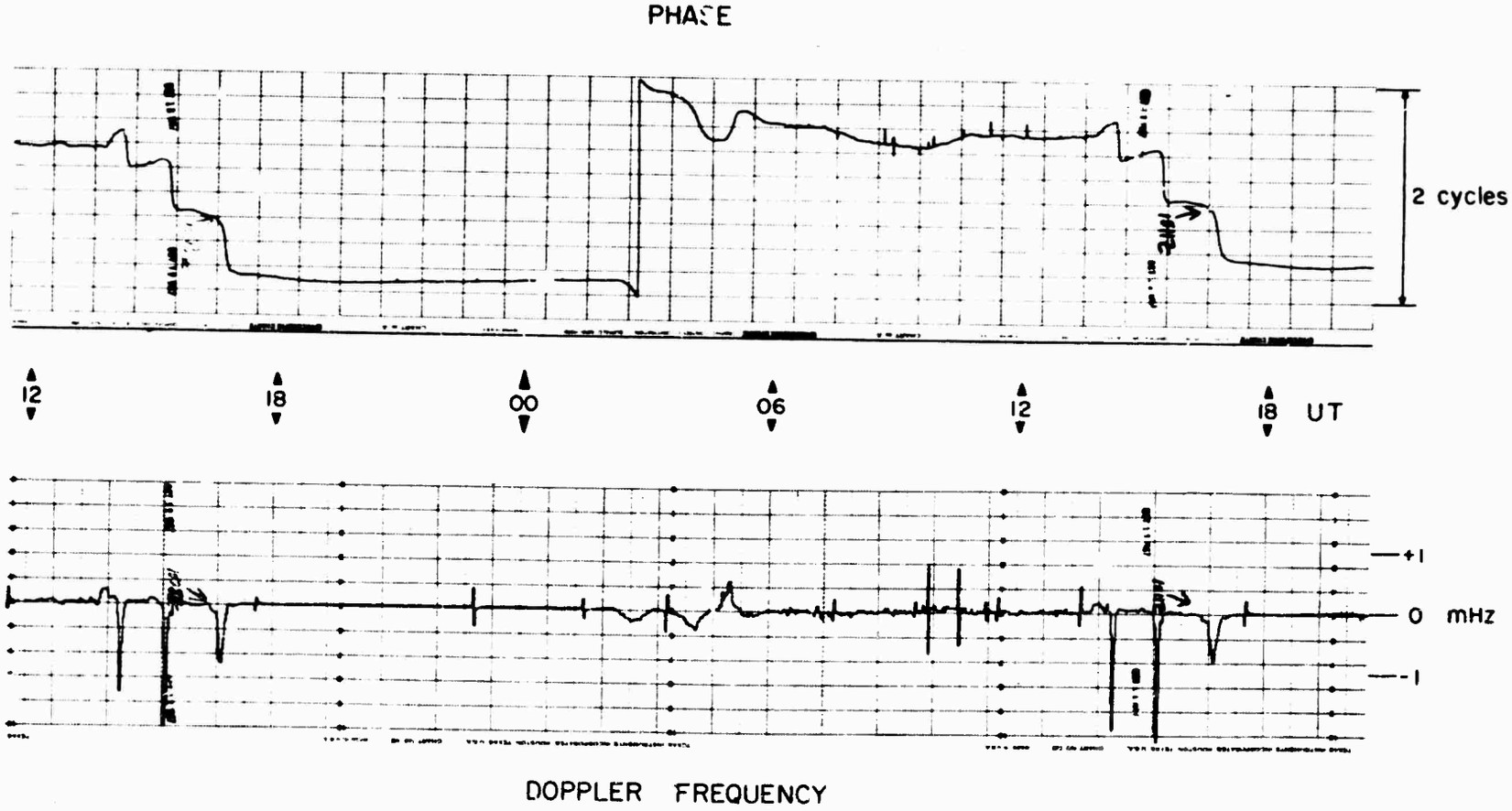


FIGURE 14

EXAMPLE OF VLF PHASE AND DOPPLER FREQUENCY RECORDS
TAKEN WITH THE DIGITAL PHASE SERVO UNIT
Rugby GBR 16 kHz Received at Boulder, Colorado
October 19-20, 1967

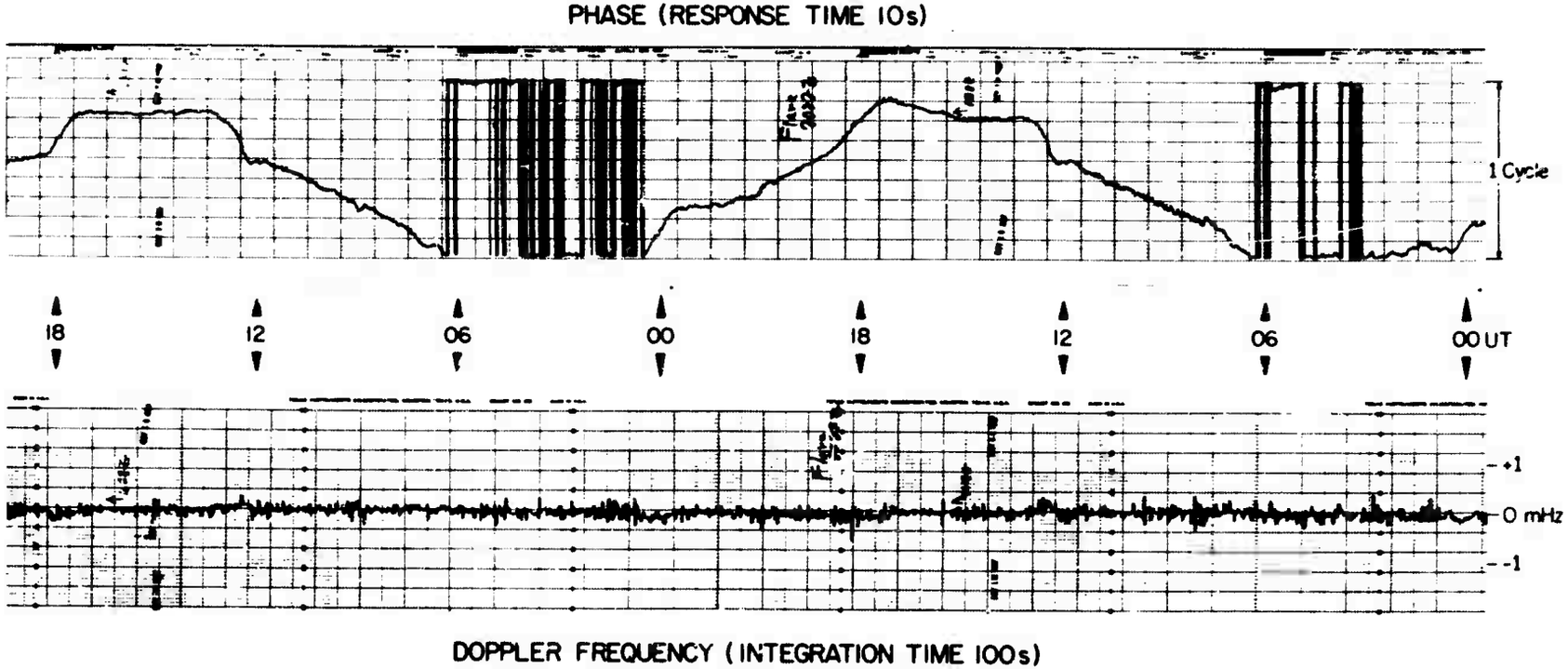


Fig. 15